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EXAMINER	
SAVLA, ARPAN P	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/824,504	MORITA ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action is in response to Applicant's communication filed November 25, 2008 in response to the Office action dated June 25, 2008. Claims 11-22 have been canceled. New claims 23-40 have been added. Claims 23-40 are pending in this application.

OBJECTIONS

Claims

1. In view of Applicant's amendment, the objections to **claims 15-19** are withdrawn.

2. **Claim 23** is objected to because the "and" at the end of line 6 should be deleted.

3. **Claim 24** is objected to because there should be a comma at the end of line 1.

4. will interpret the limitation to read "said synchronous dynamic memory."

5. **Claim 27** is objected to because the first instance of the limitation "DRAM" on line 5 should instead read "dynamic random access memory (DRAM)"

6. **Claim 27** is also objected to because the "and" at the end of line 8 should be deleted.

7. **Claim 31** is objected to because the first instance of the limitation "CPU" on line 2 should instead read "central processing unit (CPU)"

8. **Claim 31** is also objected to because the limitation "said external memory" on line 15 should instead read "said external synchronous memory."

9. **Claim 31** is also objected to because there should be a comma between the words “request” and “wherein” on line 19.

10. **Claim 33** is objected to because the limitation "said external memory" on line 3 should instead read “said external synchronous memory.”

11. **Claim 34** is objected to because the limitation "said external memory" on line 3 should instead read “said external synchronous memory.”

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112

12. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

13. **Claims 23-30 and 35-40** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

14. **As per claim 23**, the claim recites the limitation “said display unit” on line 5, however, there is insufficient antecedent basis for this limitation in the claim. Applicant may consider amending to the claim to instead read “a display unit.” For the purposes of examining the instant application, the Examiner will interpret the limitation to read “a display unit.”

15. **As per claim 24**, the claim recites the limitation “said external memory” on line 5, however, there is insufficient antecedent basis for this limitation in the claim. Applicant may consider amending to the claim to instead read “said synchronous dynamic

memory." For the purposes of examining the instant application, the Examiner will interpret the limitation to read "said synchronous dynamic memory."

16. **As per claim 27**, the claim recites the limitation "said external memory" on line 14, however, there is insufficient antecedent basis for this limitation in the claim. Applicant may consider amending to the claim to instead read "said external synchronous DRAM." For the purposes of examining the instant application, the Examiner will interpret the limitation to read "said external synchronous DRAM."

17. **As per claim 28**, the claim recites the limitation "said external memory" on line 3, however, there is insufficient antecedent basis for this limitation in the claim. Applicant may consider amending to the claim to instead read "said external synchronous DRAM." For the purposes of examining the instant application, the Examiner will interpret the limitation to read "said external synchronous DRAM."

18. **As per claim 29**, the claim recites the limitation "operable to access for read out of data" on line 2, however, this limitation is vague and indefinite. Based on line 4 of the same claim, Applicant may consider amending to the claim to instead read "operable to access read out data." For the purposes of examining the instant application, the Examiner will interpret the limitation to read "operable to access read out data."

19. **As per claim 35**, the claim recites the limitation "said external memory" on line 1, however, there is insufficient antecedent basis for this limitation in the claim. Applicant may consider amending to the claim to instead read "said synchronous dynamic memory." For the purposes of examining the instant application, the Examiner will interpret the limitation to read "said synchronous dynamic memory."

20. **As per claim 40**, the claim recites the limitation "said display unit" on line 5, however, there is insufficient antecedent basis for this limitation in the claim. Applicant may consider amending to the claim to instead read "a display unit." For the purposes of examining the instant application, the Examiner will interpret the limitation to read "a display unit."

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. Claims 23-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jones et al. (U.S. Patent 6,233,661) (hereinafter "Jones") in view of Somaya, Deepak and Linden, Greg, "System-on-a-Chip Integration in the Semiconductor Industry: Industry Structure and Firm Strategies" (hereinafter "Somaya").

23. **As per claim 23**, Jones discloses a system comprising:

a central processing unit (col. 5, lines 6-10; Fig. 2, element 102);

and a memory controller for controlling a synchronous dynamic memory (col. 5, lines 57-61; col. 7, lines 38-40; col. 8, lines 55-63; Fig. 3, element 140; Fig. 2, element 106),

wherein said memory controller is operable to receive an access request from said central processing unit or a display unit to said synchronous dynamic memory (col. 9, lines 56-60; Fig. 4A, element 304) having a data storage area divided into a plurality of banks (col. 12, lines 35-38; Fig. 4B, element 106),

wherein said memory controller is operable to provide an active command for one of said banks to said synchronous dynamic memory, based on said access request (col. 16, lines 1-15; Fig. 7, "activate command A"),

wherein said memory controller is operable to provide a precharge command for another of said banks, which is to be accessed after said one of said banks, to said synchronous dynamic memory, said precharge command being provided after providing said active command (col. 13, lines 35-39; col. 16, lines 1-15; Fig. 7, "precharge command B"),

and wherein said memory controller is operable to provide a read command or a write command for said one of said banks to said synchronous dynamic memory based on said access request (col. 16, lines 1-15; Fig. 7, "write command A"),

wherein said read command or said write command for said one of said banks is provided after said precharge command is provided for said another of said banks (col. 13, lines 35-39; col. 16, lines 1-15; Fig. 7).

Jones does not disclose that the system is an LSI.

Somaya discloses a system-on-a-chip (pg. 3). *It should be noted that a Somaya's "system-on-a-chip" is equivalent to Applicant's "LSI."*

Jones and Somaya are analogous art because they are from the same field of endeavor, that being computer systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate Jones' CPU and memory controller as Somaya's system-on-a-chip.

The motivation for doing so would have been to increase operating speeds, lower power consumption, reduce the size and complexity of end-use products, lower unit manufacturing costs, and improve system reliability (Somaya, pg. 4).

24. **As per claim 24**, the combination of Jones/Somaya discloses data of said central processing unit is stored in said synchronous dynamic memory (Jones, col. 5, lines 53-57; col. 6, lines 61-63).

25. **As per claim 25**, the combination of Jones/Somaya discloses said memory controller is operable to provide a RAS signal, a CAS signal, a WE signal and an address signal to said synchronous dynamic memory synchronized with a clock signal, and to provide said active command and said precharge command based on a predetermined combination of said RAS signal, said CAS signal, said WE signal to said synchronous dynamic memory (Jones, col. 15, lines 16-29; Fig. 8). *It should be noted the "CS (chip select)" is analogous to the "address signal."*

26. **As per claim 26**, the combination of Jones/Somaya discloses said memory controller is operable to provide address signals including a bank address signal, and a row address signal or a column address signal, to said synchronous dynamic memory synchronized with a clock signal (Jones, col. 10, lines 21-26).

27. **As per claim 35**, the combination of Jones/Somaya discloses data of said display unit is stored in said synchronous dynamic memory (Jones, col. 5, lines 53-57; col. 6, lines 61-63).

28. **As per claim 36**, the combination of Jones/Somaya discloses said memory controller is operable to provide said precharge command, after receiving said access request from said display unit (Jones, col. 13, lines 35-39; col. 16, lines 1-15; Fig. 7, "precharge command B").

29. **As per claim 37**, the combination of Jones/Somaya discloses said memory controller is operable to provide address signals including a bank address (Jones, col. 10, lines 21-26; col. 15, lines 16-29; Fig. 8),

wherein a bank address outputted with said active command is the same as a bank address outputted with said read command or said write command (Jones, col. 10, lines 21-26; col. 15, lines 16-29; Fig. 8),

and wherein a bank address outputted with said precharge command is an address of said another of said banks to be accessed, wherein said read command or said write command for said one of said banks is provided after said precharge command is provided for said another of said banks (Jones, col. 10, lines 21-26; col. 15, lines 16-29; Fig. 8; col. 13, lines 35-39; col. 16, lines 1-15; Fig. 7, "precharge command B").

30. **As per claim 27**, Jones discloses a system comprising:

a central processing unit to execute data processing (col. 5, lines 6-10; Fig. 2, element 102);

a display unit to output image data (col. 5, lines 62-63; Fig. 2, element 116);

and a memory control unit operable to read access or write access to an external synchronous dynamic random access memory (DRAM) (col. 5, lines 57-61; col. 7, lines 38-40; col. 8, lines 55-63; Fig. 3, element 140; Fig. 2, element 106) having a data storage area divided into a plurality of banks (col. 12, lines 35-38; Fig. 4B, element 106),

wherein said memory control unit is operable to receive an access request from said central processing unit or said display unit to said synchronous DRAM (col. 9, lines 56-60; Fig. 4A, element 304),

wherein said memory control unit is operable to provide an active command for one of said banks to said synchronous DRAM, based on said access request (col. 16, lines 1-15; Fig. 7, “activate command A”),

wherein said memory control unit is operable to provide a precharge command for another of said banks, which is to be accessed after said one of said banks, to said synchronous DRAM, said precharge command being provided after providing said active command (col. 13, lines 35-39; col. 16, lines 1-15; Fig. 7, “precharge command B”),

wherein said memory control unit is operable to provide a read command or a write command for said one of said banks to said synchronous dynamic memory based on said access request (col. 16, lines 1-15; Fig. 7, “write command A”),

and wherein said read command or said write command for said one of said banks is provided after said precharge command is provided for said another of said banks (col. 13, lines 35-39; col. 16, lines 1-15; Fig. 7).

Jones does not disclose that the system is an LSI.

Somaya discloses a system-on-a-chip (pg. 3).

Jones and Somaya are analogous art because they are from the same field of endeavor, that being computer systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate Jones' CPU and memory controller as Somaya's system-on-a-chip.

The motivation for doing so would have been to increase operating speeds, lower power consumption, reduce the size and complexity of end-use products, lower unit manufacturing costs, and improve system reliability (Somaya, pg. 4).

31. **As per claim 28**, the combination of Jones/Somaya discloses said memory control unit is operable to provide a RAS signal, a CAS signal, a WE signal and an address signal to said external synchronous DRAM synchronized with a clock signal, and to provide said active command and said precharge command based on a predetermined combination of said RAS signal, said CAS signal, said WE signal to said synchronous dynamic memory (Jones, col. 15, lines 16-29; Fig. 8).

32. **As per claim 29**, the combination of Jones/Somaya discloses said central processing unit is operable to access read out data stored in said external synchronous DRAM (col. 6, lines 61-63),

and wherein said display unit is operable to access read out data stored in said external synchronous DRAM (col. 6, lines 61-63).

33. **As per claim 30**, the combination of Jones/Somaya discloses said memory control unit is operable to provide access signals, including a bank address signal and an address signal, to said external synchronous DRAM synchronized with clock signals (Jones, col. 10, lines 21-26; col. 15, lines 16-29).

34. **As per claim 38**, the combination of Jones/Somaya discloses said memory control unit is operable to provide said precharge command, after receiving said access request from said display unit (Jones, col. 13, lines 35-39; col. 16, lines 1-15; Fig. 7, "precharge command B").

35. **As per claim 39**, the combination of Jones/Somaya discloses said memory control unit is operable to provide address signals including a bank address (Jones, col. 10, lines 21-26; col. 15, lines 16-29; Fig. 8),

wherein a bank address outputted with said active command is the same as a bank address outputted with said read command or said write command (Jones, col. 10, lines 21-26; col. 15, lines 16-29; Fig. 8),

and wherein a bank address outputted with said precharge command is a bank address of said another of said banks to be accessed after said one of said banks, (Jones, col. 10, lines 21-26; col. 15, lines 16-29; Fig. 8).

36. **As per claim 31**, Jones discloses a system comprising:

a central processing unit (CPU) to execute data processing (col. 5, lines 6-10; Fig. 2, element 102);

a display processing unit to output image data (col. 5, lines 62-63; Fig. 2, element 116);

and a memory controller to access an external synchronous memory synchronized with clock signals (col. 5, lines 57-61; col. 7, lines 38-40; col. 8, lines 55-63; Fig. 3, element 140; Fig. 2, element 106),

wherein said memory controller is operable to receive an access request from said CPU or said display unit to said external synchronous memory (col. 9, lines 56-60; Fig. 4A, element 304),

wherein said external synchronous memory includes a data storage area divided into a plurality of banks (col. 12, lines 35-38; Fig. 4B, element 106),

wherein said memory controller is operable to provide an active command for one of said banks to said external synchronous memory, based on said access request (col. 16, lines 1-15; Fig. 7, “activate command A”),

wherein said memory controller is operable to provide a precharge command for another of said banks, which is to be accessed after said one of said banks, to said external synchronous memory, said precharge command being provided after providing said active command (col. 13, lines 35-39; col. 16, lines 1-15; Fig. 7, “precharge command B”),

and wherein said memory controller is operable to provide a read command or a write command for said one of said banks to said external synchronous memory based on said access request (col. 16, lines 1-15; Fig. 7, “write command A”), wherein said read command or said write command for said one of said banks is provided after said precharge command is provided for said another of said banks (col. 13, lines 35-39; col. 16, lines 1-15; Fig. 7).

Jones does not disclose that the system is an LSI.

Somaya discloses a system-on-a-chip (pg. 3).

Jones and Somaya are analogous art because they are from the same field of endeavor, that being computer systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate Jones' CPU and memory controller as Somaya's system-on-a-chip.

The motivation for doing so would have been to increase operating speeds, lower power consumption, reduce the size and complexity of end-use products, lower unit manufacturing costs, and improve system reliability (Somaya, pg. 4).

37. **As per claim 32**, the combination of Jones/Somaya discloses data of said CPU is stored in said external synchronous memory (Jones, col. 5, lines 53-57; col. 6, lines 61-63).

38. **As per claim 33**, the combination of Jones/Somaya discloses said memory controller is operable to provide a RAS signal, a CAS signal, a WE signal and a bank address signal to said external synchronous dynamic memory synchronized with clock signals (Jones, col. 15, lines 16-29; Fig. 8).

39. **As per claim 34**, the combination of Jones/Somaya discloses said memory controller is operable to provide a bank address signal and an address signal to said external memory synchronized with said clock signals (Jones, col. 10, lines 21-26; col. 15, lines 16-29).

40. **As per claim 40**, Jones discloses a system comprising:

a central processing unit (col. 5, lines 6-10; Fig. 2, element 102);

a memory controller for controlling a synchronous dynamic memory (col. 5, lines 57-61; col. 7, lines 38-40; col. 8, lines 55-63; Fig. 3, element 140; Fig. 2, element 106),

wherein said memory controller is operable to receive an access request from said central processing unit or a display unit to said synchronous dynamic memory (col. 9, lines 56-60; Fig. 4A, element 304) having a data storage area divided into a plurality of banks (col. 12, lines 35-38; Fig. 4B, element 106),

wherein said memory controller is operable to provide an active command for one of said banks to said synchronous dynamic memory, based on said access request (col. 16, lines 1-15; Fig. 7, "activate command A"),

means for permitting access to another of said banks, which is to be accessed after said one of said banks, even if a mishit occurs as to access to said one of said banks (col. 13, lines 35-39; col. 16, lines 1-15) *It should be noted that Applicant's specification appears to define this means as a memory controller. Jones' memory controller is equivalent to Applicant's memory controller.*

said means comprising:

said memory controller being operable to provide a precharge command for another of said banks, which is to be accessed after said one of said banks, to said synchronous dynamic memory, said precharge command being provided after providing said active command (col. 13, lines 35-39; col. 16, lines 1-15; Fig. 7, "precharge command B"), and said memory controller being operable to provide a read command or a write command for said one of said banks to said synchronous dynamic memory

based on said access request (col. 16, lines 1-15; Fig. 7, "write command A"), said read command or said write command for said one of said banks is provided after said precharge command is provided for said another of said banks (col. 13, lines 35-39; col. 16, lines 1-15; Fig. 7).

Jones does not disclose that the system is an LSI.

Somaya discloses a system-on-a-chip (pg. 3).

Jones and Somaya are analogous art because they are from the same field of endeavor, that being computer systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate Jones' CPU and memory controller as Somaya's system-on-a-chip.

The motivation for doing so would have been to increase operating speeds, lower power consumption, reduce the size and complexity of end-use products, lower unit manufacturing costs, and improve system reliability (Somaya, pg. 4).

Response to Arguments

41. Applicant's arguments filed November 25, 2008 with respect to **claims 23-40** have been fully considered but they are not persuasive.

42. With respect to Applicant's argument regarding a memory controller providing a specific sequence of commands, which appear on pages 9-11 of the communication filed November 25, 2008, the Examiner respectfully disagrees. The term "operable to" renders the limitations dealing with "providing a specific sequence of commands" in

claims 23-40 as merely recitations of intended use of the claimed memory controller/memory control unit. A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See MPEP 2111.04. In the case of the instant application, Jones' memory controller is at least capable of providing the specific sequence of commands as done by Applicant's claimed memory controller/memory control unit (i.e. Jones' memory controller is at least capable of performing the intended use of Applicant's claimed memory controller/memory control unit). Accordingly, the combination of Jones/Somaya sufficiently meets claims 23-40.

43. As for Applicant's arguments with respect to the dependent claims, the arguments rely on the allegation that the independent claims are allowable and therefore for the same reasons the dependent claims are allowable. However, as addressed above, the independent claims are not allowable, thus, Applicant's arguments with respect to the dependent claims are not persuasive.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 23-40** have received an action on the merits and are subject of a final action.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Arpan Savla/
Examiner, Art Unit 2185
March 9, 2009

/Sanjiv Shah/
Supervisory Patent Examiner, Art Unit 2185